**2020-21**

**Q1. Describe the structure of SRAM. Distinguish among PROM, EPROM, EEPROM and Flash.**

**Answer:**

* **SRAM Structure:s**
  + SRAM (Static RAM) তৈরি হয় flip-flop circuit দিয়ে।
  + প্রতিটি cell এ 6 transistor লাগে।
  + Refresh দরকার হয় না → তাই fast, কিন্তু বেশি costly।
* **Differences:**
  + **PROM:** Programmable once only, erase possible না।
  + **EPROM:** UV light দিয়ে erase করা যায়, আবার program করা যায়।
  + **EEPROM:** Electrical signal দিয়েই erase/program করা যায়।
  + **Flash:** EEPROM এর fast version, block আকারে erase হয় (SSD, Pendrive এ use হয়)।

**Q2. Why RAM is so called?**

**Answer:**  
RAM = **Random Access Memory**  
কারণ যেকোনো memory location কে equal time এ access করা যায় → randomly, sequential না।

**Q3. Cache Mapping Problem**

A machine has:

* Main memory = 2¹⁶ bytes
* Block size = 8 bytes
* Direct mapped cache = 32 lines

**(a) How is a 16-bit memory address divided into tag, line number, and byte number?**

**Answer:**

* Byte offset bits = log₂(8) = 3 bits
* Line number bits = log₂(32) = 5 bits
* Tag bits = 16 – (5+3) = 8 bits

So: **Tag = 8 bits | Line = 5 bits | Byte offset = 3 bits**

**(b) Into what line would bytes with the address 1100 0011 0011 0100 be stored?**

**Answer:**

* Address = 1100 0011 0011 0100
* Tag = 1100 0011
* Line = 00110 = 6
* Byte offset = 100 = 4

👉 This byte stored in **Cache Line 6**.

**(c) How many total bytes of memory can be stored in the cache?**

**Answer:**

* Cache lines = 32
* Each block = 8 bytes  
  = 32 × 8 = **256 bytes**

**(d) Why is tag stored in the cache?**

**Answer:**  
কারণ একই cache line এ অনেক memory block আসতে পারে। কোন block বর্তমানে cache এ আছে তা চিনতে **Tag** লাগে।

**Q4. Give the basic elements to design different buses. Describe PCI bus structure.**

**Answer:**

* **Basic elements of bus:**
  + Data lines (data transfer করে)
  + Address lines (location specify করে)
  + Control lines (Read/Write, Clock, Interrupt)
* **PCI Bus Structure:**
  + High-speed parallel bus
  + Supports 32/64-bit data transfer
  + Plug-and-play supported
  + Used for connecting CPU ↔ I/O devices
  + Works with arbitration and synchronous clock

**Q5. Define interrupts. How do multiple interrupts managed?**

**Answer:**

* **Interrupt:** CPU execution কে থামিয়ে জরুরি কাজ (I/O request, error, signal ইত্যাদি) handle করার system।
* **Multiple interrupts management:**
  + **Priority levels:** Higher priority আগে serve হয়।
  + **Interrupt vector table:** প্রতিটি interrupt এর আলাদা routine থাকে।
  + **Masking:** কিছু interrupt temporarily disable করা যায়।

**2019-20**

**Q1. List and briefly define the possible states that define an instruction execution. (3)**

**Answer:**  
Instruction execution এ কয়েকটি ধাপ থাকে—

1. **Fetch:** Instruction টা memory থেকে আনা হয়।
2. **Decode:** Instruction টা কী কাজ করবে তা বোঝা হয়।
3. **Execute:** ALU/Control Unit instruction অনুযায়ী কাজ করে।
4. **Memory Access:** দরকার হলে memory থেকে data পড়া বা লেখা হয়।
5. **Write Back:** Result register এ store করা হয়।

**Q2. Consider a hypothetical microprocessor generating a 16-bit address (PC and address registers are 16 bits wide) and having a 16-bit data bus. (3)**

**i. What is the maximum memory address space that the processor can access directly if it is connected to a 16-bit memory?**

**Answer:**

* Address bus width = 16 → Address space = 2¹⁶ = **65,536 = 64 KB**
* Data bus = 1 6 bit → এক address এ 2 byte store হয়।
* So, max memory = **64 KB × 2 = 128 KB**

**ii. What is the maximum memory address space that the processor can access directly if it is connected to an 8-bit memory?**

**Answer:**

* Address bus width = 16 → 2¹⁶ = **64 KB**
* Data bus = 8 bit → এক address এ 1 byte।
* So, max memory = **64 KB × 1 = 64 KB**

**iii. What architectural features will allow this microprocessor to access a separate “I/O space”? If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support? How many 16-bit I/O ports? Explain.**

**Answer:**

* যদি **separate I/O instructions** (IN, OUT) থাকে, তাহলে আলাদা I/O space create হয়।
* 8-bit I/O port number = 2⁸ = **256 ports** (for 8-bit I/O ports)
* For 16-bit I/O ports → 256 ÷ 2 = **128 ports**

**Q3. Give the elements for designing bus. (1.5)**

**Answer:**  
Bus design এ তিনটা basic element থাকে:

1. **Data lines** → ডাটা transfer এর জন্য।
2. **Address lines** → কোন location থেকে ডাটা আসবে বা যাবে তা নির্ধারণ করে।
3. **Control lines** → Read/Write, clock, interrupt ইত্যাদি control করে।

**Q4. Why study Computer Organization and Architecture? Describe the structure and functions of a computer. (3)**

|  |  |  |
| --- | --- | --- |
| Feature | Computer Architecture | Computer Organization |
| Definition | **কি করে computer কাজ করে সেটা logically describe করে → functional design** | **কিভাবে hardware দিয়ে সেটা implement করা হয় → physical design** |
| Focus | **Instruction set, data types, addressing modes, CPU registers** | **Control signals, ALU, memory, buses, circuits** |
| Level | **Conceptual / Programmer view** | **Physical / Hardware view** |
| Concerned With | **Software perspective → Programmer & compiler** | **Hardware perspective → Engineer & system designer** |
| Example | **x86, ARM architecture** | **8086 microprocessor organization, cache, pipelining** |
| Change Effect | **Architecture change → software effect porda pare** | **Organization change → software unaffected, performance improve korte pare** |

**Answer:**

* **Why study COA?**
  + Computer কিভাবে কাজ করে তা বুঝতে।
  + Hardware + Software এর interaction বোঝার জন্য।
  + System performance improve করতে।
* **Structure of Computer:**
  + **Input Unit** → Data নেয়।
  + **Output Unit** → Result দেয়।
  + **Memory Unit** → Data ও Instruction store করে।
  + **Control Unit (CU)** → সব operations control করে।
  + **ALU (Arithmetic Logic Unit)** → Calculation এবং logical কাজ করে।

**Q5. Describe the evolution of DRAM and processor characteristics. (2)**

**Answer:**

* **DRAM Evolution:**
  + First generation: simple capacitor-based DRAM।
  + Later: Fast Page Mode DRAM, EDO DRAM, SDRAM, DDR, DDR2, DDR3, DDR4, DDR5 → প্রতি প্রজন্মে বেশি speed ও কম power consumption।
* **Processor Characteristics:**
  + Clock speed increase হয়েছে (MHz → GHz)।
  + Multi-core processors এসেছে।
  + Pipelining, superscalar architecture, cache memory ব্যবহার হয়েছে।
  + Power efficiency ও parallelism উন্নত হয়েছে।

|  |
| --- |
|  |
| |  |  |  | | --- | --- | --- | | Characteristic | Meaning | Example | | Word Length | CPU একবারে কত বিট process করে | 8-bit, 32-bit CPU | | Instruction Set | CPU কী কাজ করতে পারে | ADD, SUB, MOV | | Registers | CPU-এর ভিতরে ছোট memory | AX, BX, CX, DX | | Clock Speed | CPU গতি | 3 GHz | | Bus Width | একবারে কত বিট data move | 32-bit data bus | | Addressing Capability | কত memory location address করতে পারে | 16-bit → 64 KB RAM | | Instruction Cycle | এক instruction complete হতে সময় | 4 clock cycles | | Parallelism / Pipelining | একসাথে অনেক instruction process | Modern CPU pipelining | |

**Q6. Prepare a question on semiconductor main memory and answer it yourself. (2.5)**

**Question (self-prepared):**  
What are the types of semiconductor main memory?

**Answer:**

* **RAM (Random Access Memory):**
  + **SRAM (Static RAM):** Fast, costly, cache memory তে use হয়।
  + **DRAM (Dynamic RAM):** Cheaper, refresh দরকার হয়, main memory তে use হয়।
* **ROM (Read Only Memory):**
  + PROM, EPROM, EEPROM, Flash → Non-volatile, data erase/program method আলাদা।

Set Associative Mapping Summary

* Address length = (s + w) bits
* Number of addressable units = 2s+w words or bytes
* Block size = line size = 2w words or bytes
* Number of blocks in main memory = 2s+w/2w=2s
* Number of lines in set = k
* Number of sets = v = 2d
* Number of lines in cache = m=kv = k \* 2d
* Size of cache = *k \* 2*d+wwords or bytes
* Size of tag = (s – d) bits

**📌 Example:**

ধরি —

* **Main memory size = 2¹² = 4096 words (4K words)**
* **Block size = 2² = 4 words**
* **Cache lines = 16 ( = 2⁴ )**
* **Associativity = 1 (Direct mapped cache)**

**🔹 Step by Step Calculation**

1. **Address length = (s + w) bits**
   * Main memory size = 4096 words = 2¹²
   * So, total address bits = 12 bits
   * Block size = 4 words = 2² → so, w = 2
   * Hence, s = 12 – 2 = 10
   * ✅ Address length = (s + w) = 10 + 2 = **12 bits**
2. **Number of addressable units = 2^(s+w)**  
   = 2¹² = **4096 words**
3. **Block size = line size = 2ʷ words**  
   = 2² = **4 words per block**
4. **Number of blocks in main memory = 2ˢ**  
   = 2¹⁰ = **1024 blocks**
5. **Number of lines in set = k**  
   Direct mapped → k = 1
6. **Number of sets = v = 2ᵈ**
   * Cache lines = 16 → m = 16
   * Since k = 1 → v = m/k = 16/1 = 16 → so, d = 4
   * ✅ v = 2⁴ = 16 sets
7. **Number of lines in cache = m = k·v**  
   = 1 × 16 = **16 lines**
8. **Size of cache = k × 2^(d+w)**  
   = 1 × 2^(4+2) = 2⁶ = **64 words**
9. **Size of tag = (s – d) bits**  
   = (10 – 4) = **6 bits**

**📌 Final Breakdown (Address format):**

* **Tag bits = 6**
* **Set (Index) bits = 4**
* **Block offset (Word offset) = 2**

So, **12-bit address = [Tag (6) | Set (4) | Word offset (2)]**